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CLAIMS:

What is claimed is:

1. A method in a data processing system for monitoring processing of instructions, the method comprising:
 - receiving an instruction at a processor for execution;
 - responsive to being in an enabled state, determining whether the instruction is associated with an indicator in a shadow memory; and
 - performing a selected action in response to the indicator being associated with the instruction.
2. The method of claim 1, wherein the instruction is received in an instruction cache and further comprising:
 - executing the instruction after receiving the instruction for execution.
3. The method of claim 1, wherein the determining step comprises:
 - examining a register in the processor; and
 - determining whether the register is set to indicate the enabled state.
4. The method of claim 1, wherein the selected action includes at least one of sending the instruction to a performance monitor unit, sending the instruction to a data cache, and sending the instruction to an interrupt unit.

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5. The method of claim 1, wherein the instruction is received in a bundle.
6. The method of claim 1, wherein the enabled state is enabled by setting a register in a processor.
7. The method of claim 1, wherein the shadow memory contains debugging information.
8. A method in a data processing system for monitoring access to data during execution of instructions by a processor, the method comprising:
 - responsive to being in an enabled state when a data access to a memory location occurs, determining whether the memory location is associated with an indicator in a shadow memory; and
 - performing a selected action in response to the indicator being associated with the memory location.
9. The method of claim 8, wherein the selected actions is at least one of forcing an interrupt and counting accesses to the memory location.
10. The method of claim 8, wherein the shadow memory includes a shadow word for each word of data.
11. The method of claim 8, wherein the determining step comprises:
 - examining a register in the processor; and

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determining whether the register is set to indicate the enable state.

12. A data processing system for monitoring processing⁷ of instructions, the data processing system comprising:

receiving means for receiving an instruction at a processor for execution;

determining means, responsive to being in an enabled state, for determining whether the instruction is associated with an indicator in a shadow memory; and

performing means for performing a selected action in response to the indicator being associated with the instruction.

13. The data processing system of claim 12, wherein the determining means is a first determining means and further comprises:

examining means for examining a register in the processor; and

second determining means for determining whether the register is set to indicate the enabled state.

14. The data processing system of claim 12, wherein the selected action includes at least one of sending the instruction to a performance monitor unit, sending the instruction to a data cache, and sending the instruction to an interrupt unit.

15. The data processing system of claim 12, wherein the instruction is received in a bundle.

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16. A data processing system for monitoring access to data during execution of instructions by a processor, the data processing system comprising:

determining means, responsive to being in an enabled state when a data access to a memory location occurs, for determining whether the memory location is associated with an indicator in a shadow memory; and

performing means for performing a selected action in response to the indicator being associated with the memory location.

17. The data processing system of claim 16, wherein the selected actions is at least one of forcing an interrupt and counting accesses to the memory location.

18. The data processing system of claim 16, wherein the shadow memory includes a shadow word for each word of data.

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19. A computer program product in a computer readable medium for monitoring processing of instructions, the computer program product comprising:

first instructions for receiving an instruction at a processor for execution;

second instructions, responsive to being in an enabled state, for determining whether the instruction is associated with an indicator in a shadow memory; and

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third instructions for performing a selected action in response to the indicator being associated with the instruction.

20. The computer program product of claim 19, wherein the second instruction comprises:

first sub-instructions for examining a register in the processor; and

second sub-instructions for determining whether the register is set to indicate the enabled state.

21. The computer program product of claim 19, wherein the selected action includes at least one of sending the instruction to a performance monitor unit, sending the instruction to a data cache, and sending the instruction to an interrupt unit.

22. The computer program product of claim 19, wherein the instruction is received in a bundle.

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23. A computer program product in a computer readable for monitoring access to data during execution of instructions by a processor, the computer program product comprising:

first instructions, responsive to being in an enabled state when a data access to a memory location occurs, for determining whether the memory location is associated with an indicator in a shadow memory; and

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second instructions for performing a selected action in response to the indicator being associated with the memory location.

24. The computer program product of claim 23, wherein the selected actions is at least one of forcing an interrupt and counting accesses to the memory location.

25. The computer program product of claim 23, wherein the shadow memory includes a shadow word for each word of data.